

Notice of Allowability

Application No.

10/738,449

Examiner

Khanh B. Duong

Applicant(s)

NOBLE, WENDELL P.

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the filing of the application on December 16, 2003.
2. ☒ The allowed claim(s) is/are 1-25.
3. ☒ The drawings filed on 16 December 2003 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).


* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date 12/16/03 & 7/7/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.


AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

This office action is in response to the filing of the application on December 16, 2003.

Accordingly, claims 1-25 are pending.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on December 16, 2003 and July 7, 2004 are being considered by the examiner.

Allowable Subject Matter

Claims 1-25 are allowed.

The following is an examiner's statement of reasons for allowance: none of the prior art of record, taken alone or in combination, fairly shows all the limitations as claimed.

Re claim 1, none of the prior art of record discloses: forming a vertical write transistor having multiple sides, the vertical write transistor having a gate, a body region and first and second source/drain regions; forming a vertical read transistor having multiple sides, the vertical read transistor having a body region and first and second source/drain regions, the vertical read transistor further having a gate region that couples to the second source/drain region of the vertical write transistor; forming a charge storage node coupled to the second source/drain region of the vertical write transistor; forming a write bit line that couples to the first source/drain region of the vertical write transistor; forming a write wordline that couples to the gate region of the vertical write transistor; forming a read bit line that couples to the first source/drain region of the vertical read transistor; and forming a read wordline that couples to the second source/drain region of the vertical read transistor.

Re claim 9, none of the prior art of record discloses: forming multiple vertical pillars of single crystalline semiconductor material extending outwardly from the substrate, the pillars having multiple sides, each pillar including a pair of transistors in the same pillar, each of the transistors having a body region, a gate region and first and second source/drain regions, and wherein the second source/drain region of a first transistor comprises the gate for a second transistor, and wherein the first source/drain region of the second transistor comprises the body region of the first transistor, the pillars forming an array of rows and columns; forming a number of write wordlines, wherein each write wordline is coupled to the gates of the first transistors in a row of vertical pillars in the array; forming a number of write bit lines, wherein each write bit line is coupled to the first source/drain regions of the first transistors in a column of vertical pillars in the array; forming a charge storage node coupled to the second source/drain region of each first transistor in the array of vertical pillars; forming a number of read bit lines, wherein each read bit line is coupled to the first source/drain regions of the second transistors in a row of vertical pairs in the array; and forming a number of read wordlines, wherein each read wordline is coupled to the second source/drain regions of the second transistors in a column of vertical pillars in the array.

Re claim 14, none of the prior art of record discloses: forming a number of vertical pillars having an array of rows and columns, each vertical pillar comprising a vertical write transistor and a vertical read transistor each having a body region, a gate region, and first and second source/drain regions; forming a number of write wordlines, wherein each write wordline is coupled to the gates of the write transistors in one row of vertical pillars in the array; forming a number of write bit lines, wherein each write bit line is coupled to the first source/drain regions

of the write transistors in one column of vertical pillars in the array; forming a number of charge storage nodes, wherein each charge storage node is coupled to the second source/drain region of each write transistor in the array of vertical pillars, and wherein a charge stored on each of the charge storage nodes controls a conductivity of each of the read transistors in the array of vertical pillars; forming a number of independent read bit lines for nondestructive read operations, wherein each independent read bit line is coupled to the first source/drain regions of the read transistors in one row of vertical pillars in the array; and forming a number of read wordlines, wherein each read wordline is coupled to the second source/drain regions of the read transistors in one column of vertical pillars in the array, wherein each gain memory cell of the gain memory cell array has an area substantially equal to four lithographic features.

Re claim 18, none of the prior art of record discloses: forming a memory array, wherein the forming of the memory array includes forming multiple vertical pillars of single crystalline semiconductor material extending outwardly from the substrate, the pillars having multiple sides, each pillar including a pair of transistors in the same pillar, each of the transistors having a body region, a gate region and first and second source/drain regions; forming a number of write wordlines, wherein each write wordline is coupled to the gates of the first transistors in a row of vertical pillars in the array; forming a number of write bit lines, wherein each write bit line is coupled to the first source/drain regions of the first transistors in a column of vertical pillars in the array; forming a number of charge storage nodes coupled to the second source/drain region of each first transistor in the array of vertical pillars; forming a number of read bit lines, wherein each read bit line is coupled to the first source/drain regions of the second transistors in a row of vertical pairs in the array; and forming a number of read wordlines, wherein each read wordline

is coupled to the second source/drain regions of the second transistors in a column of vertical pillars in the array; forming a number of bit line drivers coupled to the respective read and write bit lines; and forming a number of wordline drivers coupled to the respective read and write wordlines.

Re claim 24, none of the prior art of record discloses: forming a number of vertical pillars forming an array of rows and columns, each vertical pillar having a vertical write transistor and a vertical read transistor each having a body region, a gate region, and first and second source/drain regions; forming a number of plate capacitors that surrounds each vertical pillar adjacent to the second source/drain region of the write transistor, wherein each plate capacitor is coupled to the second source/drain region of each write transistor in the vertical pillars, and wherein a charge stored on each of the plate capacitors controls a conductivity of each of the read transistors in the vertical pillars; forming a number of independent read bit lines for nondestructive read operations, wherein each independent read bit line is coupled to the first source/drain regions of the read transistors in one row of the vertical pillars; forming a number of read wordlines, wherein each read wordline is coupled to the second source/drain regions of the read transistors in one column of the vertical pillars; forming a read bit line driver coupled to each of the read bit lines; forming a read wordline driver coupled to each of the read wordlines; forming a number of input/output controls coupled to certain ones of the read bit lines and wordlines; forming a read bit line decoder operatively coupled to the read bit line driver; and forming a read wordline decoder operatively coupled to the read wordline driver.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

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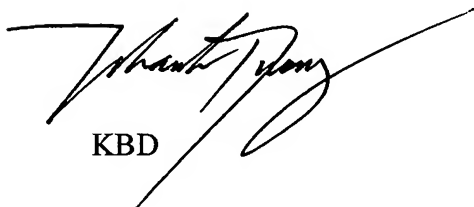
fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh B. Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on 10:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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